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A NOVEL METHOD FOR SMALL DELAY DEFECT DETECTION USING GLITCH DETECTOR

Ms.P. Anjusha
Electronics and Communication Engineering
Vivekanandha College of Engineering for Women
Tiruchengode, Erode, Tamilnadu, India.

Mrs. S. Jayachitra
Electronics and Communication Engineering
Vivekanandha College of Engineering for Women
Tiruchengode, Erode,Tamilnadu, India

Abstract— In this paper, we proposed a unified capture scheme for both small delay defect detection (SDD) and online aging prediction. A unified capture scheme can be easily incorporated into the original clock distribution system in the chip. We are introducing a new method to detect the small delay defects without using faster than at speed clock. It will significantly reduce the test power issues. A novel testing strategy can be proposed that is designed to detect small delay defects by creating internal signal races. The races are created by launching transitions along the two paths simultaneously, a reference path and a test path. The arrival time of the transitions on a common or convergence gate will determine the result of the race. The presence of a small delay defect on the test path creates a static hazard on the convergence gate that is directed to the input of a scan –latch. A glitch detector is added to the scan latch to record the presence or absence of the glitch.

Keywords— Small Delay Defect, Online Aging Prediction, Internal Signal Races, Unified Capture, Faster than at Speed Test.

I. INTRODUCTION

Over the years of ICs development, the integrated circuit technology has brought great progress to the design of high performance systems. Many challenges in the manufacturing process had to be solved to achieve this. One of the steps in this process, namely testing, is posing the most significant challenge to contemporary and future Integrated Circuit (IC) manufacturing.

Recent technology generations display a noticeable increase in delay defects that impact circuit timing. Such defects are commonly caused by gate oxide failures and resistive opens in the via and interconnect [1]. Research interest has specially focused on small (fine) delay defects, which can often remain hidden within circuit timing slacks and timing margins during testing. While it is sometimes argued that such defects, not detectable at the rated clock speed during test, are functionally benign and can be ignored, there is an emerging consensus that small delay defects can result in functional and/or reliability failures in the field. Such defects must be detected to ensure acceptable product quality and reliability in high end ICs.

A class of defects called small delay defects do not cause sufficient delay increments to cause timing failures and hence escape detection when the traditional delay test methods are used. These could be latent defects that cause failures in the field and hence are potential reliability hazards. For instance, there could be a partial open which would increase any path delay by 10–15%, but the path could still meet timing. A chip with such a defect is very likely to increase the Defects per Million (DPM). The needs to detect these small-delay defects is compounded by the fact that interconnect defects are becoming more prevalent in modern VLSI circuit.

Small Delay Defects (SDDs), which commonly arise from resistant opens and shorts, gate oxide failure, via voids, etc., have become a serious problem in integrated circuits. SDDs can cause timing failure when they are activated on a longer path during functional operation [2]. Moreover, SDDs are also a threat to circuit reliability because such defects may be magnified by the subsequent aging in the field, resulting in permanent device failure. It is essential to detect SDDs in the chip during the fabrication testing stage itself. SDDs will still be hidden because of the large timing slack of the short paths under the functional clock, thereby escaping the test stage. One of the effective ways to detect SDDs is by exploiting faster-than-at-speed testing. By increasing the test clock frequency, timing slackness of the short paths decreases, which improves the capability of screening SDDs.

Delay testing is the most effective method for detecting resistive interconnects defects. The primary challenge in detecting small-delay defects is that the delay increment caused by these defects is less than the path slack and traditional delay test methods only detect defects that are greater than the slack interval. Thus detecting defects which

cause small delay increments requires faster than at-speed clock frequencies.

Aging effects have become a prominent reliability challenge as the process advances into the nanometer regime. Much work has been done on understanding and modeling the intrinsic mechanism of aging, such as Negative/Positive Bias Temperature Instability (NBTI/PBTI), time-dependent dielectric breakdown, hot-carrier injection, electro migration, etc. Circuit aging is a gradual process; online aging prediction is an effective way to prevent the system data or state corruption from aging induced circuit failure [3]. It captures the circuit response under the normal working mode and generates a warning signal if the aging-induced delay degradation exceeds a specified threshold. Based on this warning information, some redundancy or tuning mechanisms can be enabled to ensure that the system can continue to work well.

The hardware circuit used in manufacturing testing is usually deactivated or abandoned when the chip works in the field. However, for reliability, the designer still needs to insert specific circuits for online monitoring some faults which may result in functional failure of the chip, such as soft error, inductive noise, and aging-induced delay degradation. If we can reutilize the hardware circuit designed for offline manufacturing testing to online fault detection or monitoring, the implementation complexity in defect- or aging-related reliability design can be significantly reduced. Meanwhile, the total area overhead consumed by offline and online circuits can be saved as well [4].

We noticed that SDD detection and online aging prediction have a common characteristic, i.e., both of them need to capture the circuit response ahead of the functional clock. This motivates us to propose a unified capture scheme to support both faster-than-at-speed testing and online aging prediction. It reuses the offline test hardware circuit in online monitoring of circuit aging and generates an on-chip programmable clock signal to flexibly capture the circuit response at the designated time.

However, the implementation of a unified capture scheme is confronted with some challenges. The intrinsic aging process will degrade the on-chip circuit. With the continuous reduction in oxide thickness and the increase in operational temperature, the NBTI effect can become a limiting factor in the device lifetime. The PBTI effect emerges as a dominant aging mechanism in sub-32-nm high-*k* processes. Aging effects can cause the drift in the generated clock signal and thereby result in the interval for capturing the circuit response in online aging prediction to deviate from its initial span gradually. This makes the traditional hardware circuit designed for fabrication testing unfit for online operation.

Another important design concern in the proposed clocking scheme is the negative impact of process variation (PV) on the on-chip circuit. PV will cause a skew in the generated clock signal, thus affecting the test efficiency of faster-than-at-speed testing or the prediction accuracy of online aging prediction.

We tackled the above design concerns in the proposed unified capture scheme. Our main contributions are as follows.

- It proposes a new method is to detect the very small delay defects without using faster than at speed clock. It will significantly reduce the test power issues. This novel testing strategy is useful to detect small delay defects by creating internal signal races. The races are created by launching transitions along two paths simultaneously, a reference path and a test path. The arrival times of the transitions on a common or 'convergence' gate determine the result of the race.

- It can detect the presence of a small delay defect on the test path by creating a static hazard on the output of the convergence gate that is directed to the input of a scan-latch. A glitch detector can be added to the scan latch to record the presence or absence of the glitch.

- The proposed aging-resistant design method significantly reduces the drift in the generated clock signal under runtime NBTI effect. Reversed short channel effect (RSCE) is also exploited to determine the optimal transistor channel length for the circuit design. This minimizes the skew of the generated clock signal in the presence of P V[5].

I. UNIFIED CLOCKING SCHEME

1.1 Top view

Faster-than-at-speed testing and online aging prediction have a common characteristic: both of them need to capture circuit response ahead of the functional clock. During faster-than-at-speed testing, after the test vector is applied to CUT by a launch clock, a faster capture clock is used to capture the test response. This clock reduces the timing slack of short paths, thereby improving the capability of SDD detection .Similarly, a capture interval is formed before the trigger edge of the

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functional clock during the time that online aging prediction is performed. It generally spans tens to hundreds of picoseconds. If a transition on the circuit output falls into the capture interval, it will be captured by the aging sensor and is recognized as an indication that circuit aging has exceeded the designated threshold.

The PCSGM module generates programmable clock signals which can be used as launch and capture clocks (together denoted as xCLK) for faster-than-at-speed testing as well as the control signal (CTRL) to form the capture interval for online aging prediction. Two control signals global scan enable signal (GSEN) and SEL are applied to the working mode selection module (WMSM) and the clock selection module (CSM) [6]. They are used to switch the working modes between faster-than-at-speed testing and online aging prediction as well as to select the corresponding clock signals. The AS unit is the aging sensor that generates the warning signal if a transition occurs within the specific capture interval.

In this paper, with the support of PCSGM, we propose an aging sensor with a very simple structure. The main body of the proposed aging sensor contains six transistors compared to the one proposed in with an eight-transistor configuration. A warning signal will be generated if a transition on the combination circuit output occurs within the capture interval.

When power on, GSEN and SEL both remain at logic "0," the capture circuit therefore first steps into the idle mode. In this mode, the functional clock is applied to the combination circuit (circuit under test) while the capture circuit is at the aging-resistant state.

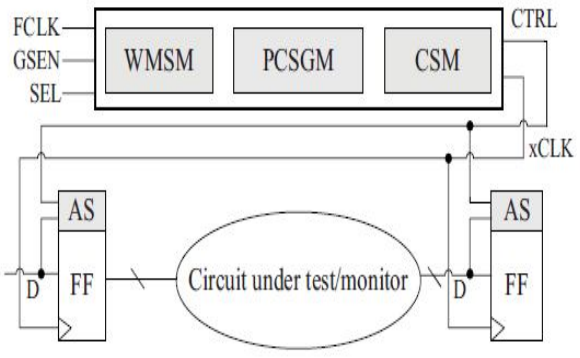

Fig 1: Framework of the proposed unified capture Scheme

The proposed system performs following operations:

2.2 Generation of Programmable Clock Signal

Two falling transition signals upper delay line (UDL) and lower delay line (LDL) are generated by the programmable delay sub module in PCSGM (shaded parts inside PCSGM).The programmable delay sub module possesses asymmetric characteristic and operates under a well designed control mode [7]. It facilitates the transformation of UDL and LDL into the clock signals to be used either in faster-than-at-speed testing or in online aging prediction. The test clock frequency or the capture interval is decided by the delay difference between the opened delay stages in the programmable delay sub module.

The programmable delay sub module is divided into the upper delay part (UDP) and the lower delay part (LDP). Each delay part consists of multiple delay stages. Each delay stage has one or more delay elements (DEs). The number of delay stages in UDP is higher than that in LDP. In any case, delay of the opened delay stages in UDP is always smaller than that in LDP. Suppose the number of delay stages on UDL and LDL is m and n, respectively, and the number of opened delay stages on UDL and LDL is p and q, respectively. The propagation delays of a single DE on UDL and LDL are denoted as TPU and TPL , respectively.

2.3 Performing Faster-Than-at-Speed Testing

During faster than- at-speed testing, the chip under test works alternatively between two modes. When GSEN and SEL both are at logic "1," the scan clock SCLK can be applied to the system clock tree to scan in the test vectors (from the scan input, SI) or scan out the test responses. When GSEN switches from logic "1" to logic "0" while SEL remains at logic "1," two falling transitions will be generated on UDL and LDL. These two falling transitions are fed into the faster-than-at-speed testing module circuit (FMC) unit and are transformed into the launch and capture clocks.

2.4 Performing Online Aging Prediction

During the normally functional operation of the chip, SEL and GSEN both remain at logic "0." At this time, the functional clock FCLK is applied to the system clock tree. For performing online prediction, SEL remains at logic "0" while GSEN switches from logic "0" to logic "1." This will trigger a rising transition on the input signal (IN) of the programmable delay sub module and a falling transition on the output signals of UDL and LDL, respectively.

UDL is inverted by INV1 which substitutes FCLK to feed the system clock tree in the aging prediction mode. LDL is NORed with the inverted UDL to generate a control signal CTRL. CTRL is fed into the aging sensors and is used to form the capture interval in online aging prediction.

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In the online aging prediction mode, SEL remains at logic "0," which prevents SCLK from applying to the FFs in LDP while organizing the FFs in UDP into a new CSR. Therefore, the segment of the control vector that lies in the FFs in UDP can be shifted circularly under the control of SCLK. This will alter the opened delay stages in the UDP and in turn will alter the capture interval in online aging prediction.

2.5 Aging-Resistant Design Concern

The hardware circuit used in online aging prediction should be aging-resistant to minimize the drift in the capture interval during the runtime usage. In this paper, we concentrate on aging-resistant design consideration of the proposed capture circuit on the BTI effects, including NBTI and PBTI. NBTI has been widely recognized as a major aging mechanism in poly-gate CMOS circuits, while PBTI is found to be dominant in high-*k* processes. Of course, there are still some other aging effects that will degrade the proposed capture circuit. However, by making the capture circuit BTI- resistant, we believe it has a good chance to maintain the operation accuracy in the runtime.

In summary, the proposed capture circuit is BTI-resistant during the long idling period. Of course, it is impossible to completely eliminate aging-induced degradation on the capture circuit, especially when it is functioning. Fortunately, the capture circuit can dynamically adjust the capture interval in the runtime. This further improves the aging-resistant capability of the capture circuit because we can adjust the capture interval back to the predefined value when the capture circuit has aged to some extent.

2.6 Implementation Problems

Here we discuss the implementation problems related to the practical operation of the capture circuit. One is how to generate and reuse the two control signals GSEN and SEL. The other is the test generation issue for faster-than-at-speed testing.

GSEN and SEL signals can be provided by the external ATE during the faster-at-speeding testing. When the chip starts service in the field, these two signals can be reused to switch the capture circuit between the idle and online aging prediction modes. We propose two simple schemes for generating GSEN and SEL in the field. First, a small MCU such as 8051 located off-chip can be used to generate GSEN and SEL and program their timings. Such an MCU usually has price below US$1 and occupies a small area of the board. The second way to generate GSEN and SEL is by constructing a very simple finite state machine (FSM) on-chip. The FSM provides only three states for the capture circuit, namely, the idle mode, the set/reset mode, and the online aging prediction mode. The set/reset mode means that before starting the operation of online aging prediction, the scannable FFs in the programmable delay sub module are first forced into a certain state (i.e., the control vector is formed correspondingly).

Circuit design for implementing faster-than-at speed testing is more or less independent of the test generation. As long as the designed test circuit can support the common modes in scan-based delay testing, such as launch-off-capture (LOC) or launch-off-shift (LOS), it can seamlessly combine with the generated test vectors and perform faster-than-at speed testing.

II. PV-RESILIENT DESIGN

PV-induced parameter variability can manifest themselves across several dies (die-to-die) or within a single die (within die).Within-die variation can be further divided into systematic and random components. Systematic variation is mainly caused by sub wavelength lithography and line-edge roughness, while the random variation arises from the fluctuation in oxide thickness and random dopant fluctuation (RDF). In earlier processes, die-to-die variations dominate the parameter variability. However, with the continuous shrinking in the feature size, within-die variations become more and more prominent.

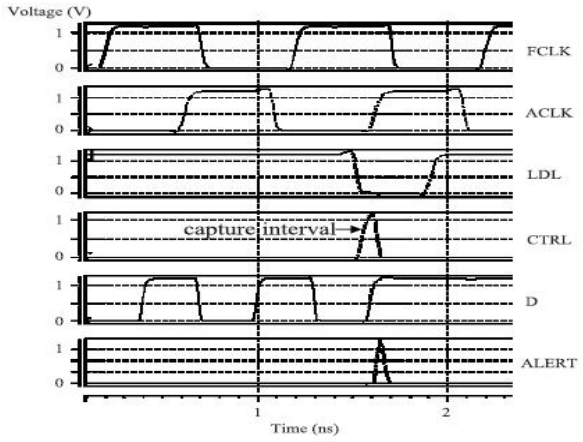

Fig.2 : Simulation waveform for online aging prediction

IV. VERIFICATION AND DISCUSSION

4.1 Online Aging Prediction

The proposed unified capture circuit is first exploited to perform online aging prediction. Fig.2 illustrates the corresponding simulation waveform. The capture interval is set

to 70 ps (i.e., bound of this capture interval is at 930 ps). As shown in Fig.2, ALERT, the output of aging sensor, remains at logic "0" even though there are two transitions on D occurring outside the capture interval. When the third transition occurs inside the capture interval, the aging sensor generates a rising transition (ALERT 0→1) as the warning signal.

4.2 Faster-Than-at-Speed Testing

Fig. 3 illustrates the simulation waveform for faster-than-at-speed testing using the LOS scheme. The simulation waveform for the LOC scheme is not presented here because it is very similar to that of LOS except LSEN can be de-asserted asynchronously. The test clock period is set to 480 ps

As shown in Fig. 3, during the scan-in phase, SCLK is applied to the clock tree to shift the test vector. GSEN is then de-asserted to enable the generation of launch and capture clocks using the programmable delay sub module. After the launch operation, LSEN is de-asserted fast to switch CUT from the scan-in mode into the functional mode. After capturing the circuit response, LSEN is asserted to logic "1" again and SCLK is applied to the clock tree to scan out the test response.

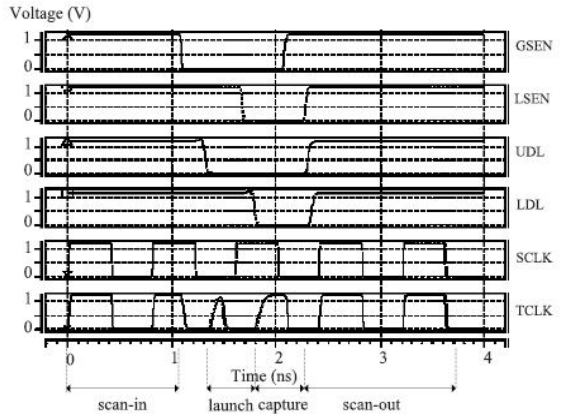

Fig. 3: Simulation waveform for Faster than at speed testing

V. CONCLUSION

In this paper, we proposed a unified capture scheme to support both the faster-than-at-speed testing and online aging prediction. A novel testing strategy is proposed that is designed to detect small delay defects by creating internal signal races. The races are created by launching transitions
The presence of a small delay defect on the test path creates a static hazard on the convergence gate that is directed to the input of a scan –latch. A glitch detector is added to the scan latch to record the presence or absence of the glitch unlike previous work, the underlying capture circuit in this paper possesses asymmetric characteristic and operates under a well-designed control mode. It can generate programmable clock signals that facilitate the achievement of different test clock frequencies in faster-than-at-speed testing as well as capture intervals in online aging prediction. Components in the underlying capture circuit are aging-resistant, which significantly reduces the drift in the capture interval caused by aging effects. By choosing the channel length of the transistor from the RSCE range, the proposed capture circuit is resilient to PV. The proposed unified capture scheme can be easily incorporated into the original clock distribution system in the chip. It just adds multiplexers in clock distribution nodes to select the corresponding clock signals giving different working modes without changing the closed form of the original clock distribution system.

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